5–6 GHz Monolithically Integrated Calibratable Low-Noise Downconverter for Smart Antenna Arrays

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Abstract — **An integrated downconverter for active antenna arrays is presented. From 5.125 GHz to 5.875 GHz the downconverter shows more than 20 dB conversion gain and a noise figure of less than 3.8 dB with a minimum of 3.3 dB. Input 1 dB compression point is -18 dBm. Image rejection better than 35 dB is achieved using an integrated lumped-element bandpass filter. A switchable symmetric input amplifier is proposed to calibrate amplitude and phase errors without degrading the noise figure.**

I. Introduction

In the last years, there has been a growing interest in multiple antenna systems. Among the potential benefits are the increase of system capacities, the reduction of intersymbol interference or higher possible data-rates using space-time *coding [1].*

With upcoming wireless LAN standards at 5–6 GHz the used wavelengths become sufficiently small to apply the smart antenna principle to mobile communication systems and portable devices. But additional to the small space needed for the antennas, those systems have to be compact, robust and producible at low prices.

Several integrated receivers have been published [2]–[4] for traditional single-channel systems. In a smart antenna system some additional requirements have to be fulfilled. Cross talk over the common feeding network has to be avoided. The local oscillator (LO) signal needs to be distributed by a dividing network, the resulting losses need to be accounted for. The active microwave components, connections, and high-order filters in the stages following the downconverter introduce different and time-varying phase and amplitude errors, which need to be determined and calibrated.

In this paper a completely monolithically integrated downconverter is presented which can be directly mounted with each antenna element without the need for additional external components. For this design, the Triquint TQTRx process was used which features 0.6 µm–MESFETs with a transit frequency of 20 GHz and suitable passive elements like spiral inductors with a quality factor Q around 20 at 5 GHz.

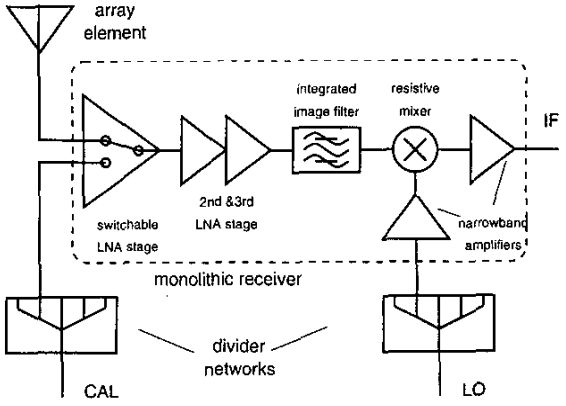

Fig. 1. Block diagram of the chip.

II. System Architecture

The block diagram in Fig. 1 shows the basic functionality of the developed circuit. A heterodyne architecture is used. One way to calibrate the downconverter is to switch between a precisely known reference signal (calibration mode) or the antenna input (receiving mode). Using a passive switch with a typical insertion loss of 1–2 dB [5] would significantly degrade the noise figure. Therefore a switchable low-noise amplifier is proposed.

The pre-amplifier is followed by an integrated image rejection filter. The high intermediate frequency of 1.45 GHz makes image filtering possible, while the "quiet" image band (LO is above RF) relaxes the requirements on the image rejection. The high-quality passive elements offered by the MMIC-process are used to perform filtering without the need of off-chip components. A passive resistive mixer, showing low noise and good linearity, is used to convert the signal down. Narrowband amplifiers are used as gain stages at IF and for the LO signal. Additionally the LO amplifier provides backward isolation.

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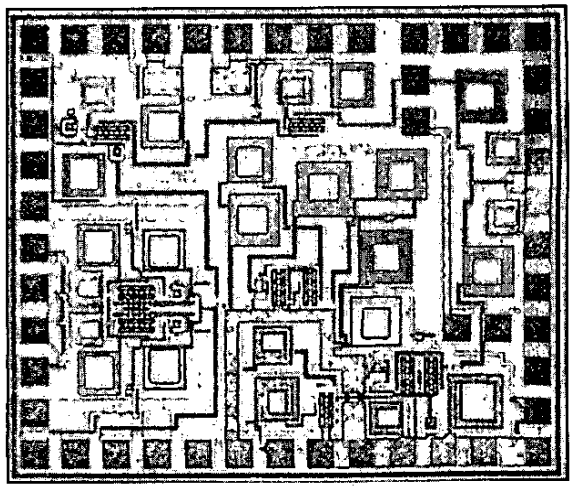

Fig. 2. Chip micrograph (Chip size is 1.95 mm×1.6 mm)

III. Circuit Design

A. Switchable LNA

The first LNA stage consists of two symmetric 300 μm enhancement FETs connected at the drains (see Fig. 3). An inductive source feedback is used to improve the linearity and increase the real part of the input impedance [6].

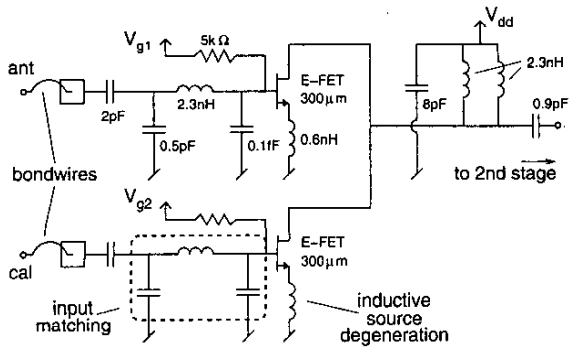

Fig. 3. Switchable LNA stage

The impedance at the connected drains is strongly dependent on the states of the two transistors. The interstage matching to the following two stages assumes that the transistors are alternatively switched. One transistor is biased for best linearity at a current density of I_d/w=40 μA/μm, the second one is switched off by setting the gate bias to V_{gs}=0 V.

Differences in gain or phase of the two parallel input stages lead to calibration errors. Therefore completely symmetric layout is used. The transistors are located very close to each other and show the same gate orientation to avoid device mismatching.

Taking into account that one switch-state might be used for a long time in receive mode, while the calibration should be possible in a comparably short interval, thermal effects on the devices need to be considered. To keep them on the same temperature, the transistors are physically connected at the drains. To get a rough estimate, the following assumption can be made: if both transistors are thermally independent and the paths of heat transportation are limited to the way down through the substrate, the working transistor will heat up due to its losses, while the other stays at room temperature. With a drain current of 7 mA at 3 V and the thermal conductivity 0.5 W/Kcm of GaAs the computed temperature difference is less than 0.1 K indicating that thermal effects can be neglected in this case.

A further crucial point is the large-signal behavior of the switch in off-state. As low-power enhancement FETs are used, strong input signals exceeding the threshold voltage V_{th} switch the transistor on, thus degrading the isolation. As the isolation at high input power levels is needed for the application in any practical system it is important to control this effect. To avoid the use of negative control voltages the transistor width was increased to lower the input impedance and therefore also the voltage swing on the gate.

This approach leads to a trade-off between maximum tolerable input power and current consumption. It is assumed that signals stronger than the aimed 1 dB input compression point do not occur, as the usual system designs imply that the receiver always works in its linear region. The device was made large enough that the isolation does not degrade below this power level of −20 dBm. Corresponding simulations were carried out using the TOM3 large-signal model [7].

B. Integrated Image Filter

The image filter consists of a third-order bandpass filter realized with lumped elements according to Fig. 4. Since the filter is sensitive to parasitics, its layout was carefully optimized.

The crucial limitations in achieving high stopband attenuation are internal coupling and the absence of good grounding. On semi-insulating GaAs substrate magnetic coupling is dominant, which was considered for the layout. To circumvent the grounding problem, filter ground and amplifier ground were separated. By providing a number of bondwires to ground the package parasitic L_p was kept sufficiently low not to degrade the stopband rejection. GSG-pads were added to permit on-wafer measurements of the filter.

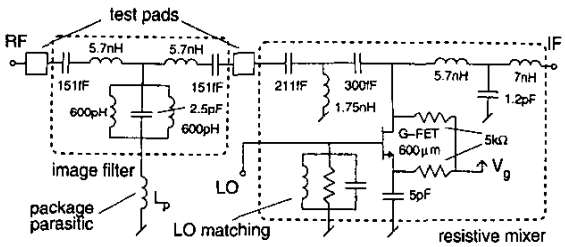

Fig. 4. Image filter and mixer

C. Resistive Mixer

Fig. 4 shows the downconverting mixer that uses a "cold" (V_{ds}=0 V) FET in the resistive region. A wide 600 µm deep-depletion FET is chosen to achieve high linearity [8]. With a signal applied on the gate, the drain shows a large-signal impedance which is convenient to match to the RF and IF ports [9]. The matching was done using a low-pass and a high-pass T-structure for IF and RF, respectively. To achieve the highest possible conversion gain, the gate is biased slightly below threshold. The gate is matched to the LO amplifier to increase the overall efficiency.

All devices are biased using integrated bias networks so that no additional off-chip connections are needed and furthermore the process variations are compensated.

IV. Experimental Results

The fabricated die was bonded on a Duroid 6010 substrate and tested. Fig. 5 shows the measured conversion gain as a function of LO power. It saturates at 26.2 dB for LO levels higher than 0 dBm.

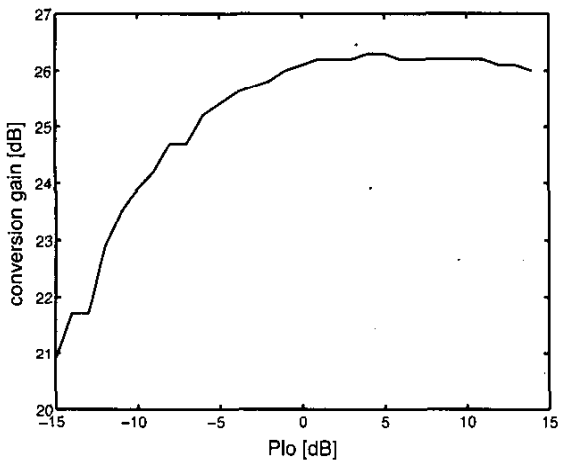

Fig. 5. Conversion gain vs. LO power level. f_{RF}=5.5 GHz, f_{IF}=1.45 GHz

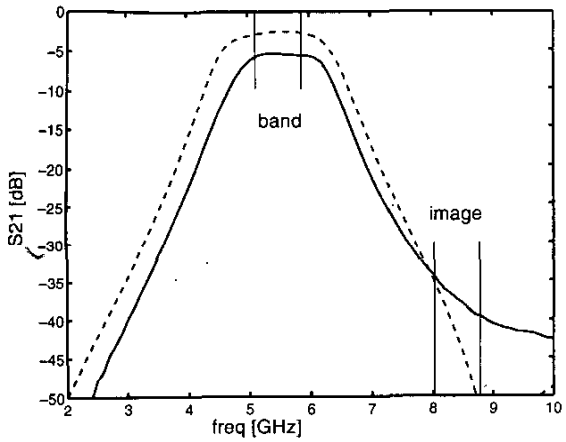

Fig. 6. Measured(—) and simulated(- -) image filter response

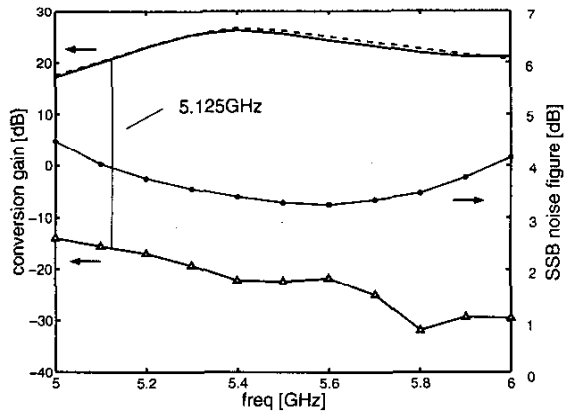

Fig. 7. Frequency response of both channels(- -/—), image(△) and noise figure(*). P_{LO}=5 dBm

Fig. 6 shows the on-wafer measurement of the integrated image-filter compared to the simulations. The measured bandwidth is smaller, but still sufficient. The filter insertion loss is 6 dB and therefore higher than simulated. The stopband attenuation is better than 35 dB.

To measure the frequency behavior of the whole chip, RF and LO frequencies were swept, keeping f_{IF}=1.45 GHz constant. The resulting curves are depicted in Fig. 7: Over the 5.125 GHz to 5.875 GHz range, the gain is above 20 dB. Image rejection is 36.7 dB at 5.125 GHz and raises to 50 dB at 5.875 GHz which is a very good result for integrated receivers. Over the interesting band the very low SSB noise figure is below 3.8 dB with a minimum of 3.3 dB at 5.6 GHz. The gain difference between the two input channels stays below 0.7 dB.

Fig. 8 shows the large input signal behavior: 1 dB gain compression occurs at an input power level of −18 dBm, which is higher than the typically needed −20 dBm for

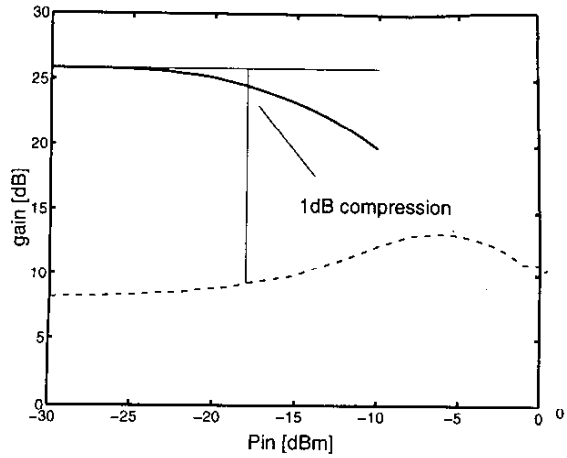

Fig. 8. Large signal behavior of selected(—) and deactivated(- -) channel at f_{RF}=5.5 GHz

WLAN applications.

The switch isolation of the LNA is 17.65 dB at low power levels, decreasing to 16.55 dB at the compression point. The expected degradation of the switch isolation occurs at input power levels higher than 15 dBm, having no practical importance. From a two-tone measurement with Δf=100 kHz the IP_3 at the input is determined to -10 dBm.

The circuit draws 55 mA for the signal path (LNA, mixer and IF amplifier) and 21 mA for the additional LO amplifiers, resulting in a total 76 mA from a 3 V supply. Fig. 2 shows the micrograph of the developed chip. Total chip size is 1.95 mm$\times$1.6 mm. In Tab. I. the circuit performance at f_{RF}=5.5 GHz is compared with the recently published results of other integrated 5–6 GHz receivers.

V. Conclusions

In this paper, the design and characterization of a one-chip monolithic downconverter for 5.125–5.875 GHz is presented. A novel switchable low-noise amplifier is proposed for system calibration. The use of passive input switches and the associated losses are avoided, thus leading to a very low system noise-figure of 3.3 dB, which, to the authors knowledge, is the lowest noise figure reached for integrated receivers in this frequency band.

The measured amplitude difference between the two input ports is smaller than 0.7 dB, allowing a calibration of the downconverter itself and all following stages.

Using on-chip image filtering, more than 35 dB rejection are obtained. Measured conversion gain is higher than 20 dB and the total power consumption is 228 mW, whereby the signal path dissipates 165 mW.

The presented downconverter is perfectly suitable for compact and inexpensive active antenna arrays.

VI. Acknowledgements

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TABLE I.

Published performances of integrated 5–6 GHz receivers

	[2]	[3]	[4]	**this work**
gain	19 dB	26 dB (vgain)	43 dB (vgain)	**26 dB**
im. rej.	>40 dB	>50 dB	62 dB	**48 dB**
$P_{in,1dB}$	−22 dBm	−18 dBm	−26.5 dBm	**-18 dBm**
NF	5.9 dB	7.2 dB	6.4 dB	**3.3 dB**

References

[1] H. Gesbert, H. Bölcskei, D. Gore, A. Paulraj, "MIMO Wireless Channels: Capacity and Performance Prediction", IEEE *Globecom 2000*, vol. 2, p. 1083

[2] M. Copeland, S. Voinigescu, D. Marchesan, P. Popescu, M. Maliepaard, "5-GHz SiGe HBT Monolithic Radio Transceiver with Tunable Filtering", *IEEE T. on Microwave Theory and Techniques*, vol. 48, no. 2, , p.170, Feb. 2000

[3] T. Lee, H. Samavati, H. Rategh, "5-GHz CMOS Wireless LANs", *IEEE T. on Microwave Theory and Techniques*, vol. 50, no. 1, p. 286, Jan. 2002

[4] B. Razavi, "A 5.2-GHz CMOS Receiver with 62-dB Image Rejection", *IEEE J. of Solid-State Circuits*, vol. 36, no. 5, p. 810, May 2001

[5] J. Alves Torres, J. Costa Freire, "Monolithic Transitors SPST Switch for L-Band", *IEEE T. on Microwave Theory and Techniques*, vol. 50, no. 1, p. 51, jan. 2002

[6] F. Heaney, F. McGrath,P. O'Sullivan, C. Kerrmarrec, "Ultra Low Power Low Noise Amplifiers for Wireless Communications", *15th Annual GaAs IC Symposium Technical Digest 1993*, p. 49, oct. 1993

[7] R. Hallgren, P. Litzenberg, "TOM3 Capacitance Model: Linking Large- and Small-Signal MESFET Models in SPICE", *IEEE T. on Microwave Theory and Techniques*, vol. 47, no. 5, p. 556, May. 1999

[8] F. Ellinger, R. Vogt, W. Bächtold, "Compact Monolithic Integrated Resistive Mixers With Low Distortion for HIPERLAN, *IEEE T. on Microwave Theory and Techniques*, vol. 50, no. 1, p. 187, Jan. 2002

[9] S. A. Maas, "Microwave Mixers", Norwood, MA, 1993